Amendments to the Claims:

Claims 1-7 (Previously cancelled).

Please cancel claims 16 and 22-28.

8. (Amended herein) A system for calibrating ~~the~~ an RC time constant of an integrated clock, comprising:

a register for storing a reset number;

a counter coupled to receive ~~a~~ the reset number from the register and further coupled to receive clock cycles from an RC oscillator;

a master counter for receiving a reset signal from the counter, which reset signal is generated by the counter whenever the number of clock cycles that is received from the RC oscillator matches the reset number received from the register;

the master counter being further coupled to receive clock signals from a master clock, which master counter generates a count value, which count value reflects the number of clock cycles received from the master clock since the last reset signal was received; and

calibration circuitry coupled to receive the count value from the master counter wherein the calibration logic generates control signals to the RC oscillator to increase or decrease the RC time constant according to the value received in the count signal from the master counter.

9. (Original) A system of claim 8 wherein the register stores a reset number that is equal to 1,000.

10. (Original) The system of claim 8 wherein the calibration circuitry generates a signal to increase the RC time constant if the value of the count number received from the master counter is greater than 1,000.

11. (Original) The system of claim 8 wherein the calibration circuitry generates a signal to decrease the RC time constant if the value of the count number received from the master counter is less than 1,000.

12. (Amended herein) The system of claim 8 wherein the calibration circuit includes logic to increase the RC time constant of the RC oscillator by generating signals to increase ~~the~~ capacitance therein.

13. (Amended herein) The system of claim 8 wherein the calibration circuit includes logic to decrease the RC time constant of the RC oscillator by generating signals to decrease ~~the~~ capacitance therein.

14. (Original) The system of claim 8 wherein the RC time constant is adjusted by switching capacitors of a capacitor array in or out of connectivity within the RC oscillator according to whether an RC time constant requires increasing or decreasing to cause the oscillator to produce a desired frequency of operation.

15. (Original) A method for adjusting an RC time constant in an oscillator, comprising:

setting a capacitor array to an initial first value of capacitance;

receiving a count value;

determining whether the RC time constant is low;

if the RC time constant is low, incrementing the capacitance value to a new value;

if the RC time constant is not low, determining the whether the RC time constant is high; ~~and~~

if the RC time constant is high, decrementing the capacitance to a new value; and.

determining if the change included a minimal step size.

16. (Cancelled)

17. (Amended herein) The method of claim ~~12~~ 15 wherein the new value is approximately one-half of the possible amount of capacitance that may be changed from a present value to a maximum value.

18. (Amended herein) The method of claim ~~12~~ 15 wherein the new value is a value that is approximately one-half of the possible amount of capacitance that may be changed from the present value to a minimum value.

19. (Original) The method of claim 15 wherein the RC time constant value is determined to be low if a count value is higher than a specified number.

20. (Original) The method of claim 15 wherein the RC time constant value is determined to be high if a count value is lower than a specified number.

21. (Original) The method of claim 15 wherein the initial value is one that is approximately half of the total amount of capacitance that may be set within the capacitor array.

22-28 (Cancelled herein).